CLAIMS

What is claimed is:

1. A method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising:

opening a window for helium implantation on a hydride vapor phase epitaxy (HVPE) grown n^+ GaN quasi-substrate layer, using optical lithography;

implanting helium on the n+ GaN quasi-substrate layer over the window for helium implantation, so as to provide an insulating layer for contact pads of the device;

opening a window for collector fingers using E-beam lithography;

depositing an ohmic metallization layer over the window for the collector fingers;

lifting-off ohmic metallization, thereby forming the collector fingers;

opening a window for a self-aligned base recess using optical lithography; and

etching to recess a base layer to an n^- GaN quasi-substrate layer grown on the n^+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage.

2. The method of claim 1 further comprising:

opening a window for a collector contact pad, using optical lithography;

depositing a high quality silicon nitride layer over the window for a collector contact pad; and

lifting-off or wet chemical etching the high quality silicon nitride layer, thereby forming a silicon nitride collector contact pad.

3. The method of claim 2 wherein the high quality silicon nitride layer is about 1000-2000Å thick, and is deposited over the window for helium implantation via plasma enhanced chemical vapor deposition (PECVD).

4. The method of claim 2 further comprising:

opening a window for Ti metallization of the collector contact pad using optical lithography;

depositing Ti over the window for Ti metallization of the collector contact pad; and

lifting-off Ti metallization, thereby forming a Ti collector contact pad.

5. The method of claim 4 further comprising:

opening a window for a second Ti metallization of the collector contact pad using optical lithography;

depositing Ti over the window for the second Ti metallization of the collector contact pad; and

lifting-off second Ti metallization, thereby forming a Ti cap over the collector contact pad.

6. The method of claim 2 wherein depositing Ti over the window for Ti metallization of the collector contact pad includes depositing Ti/Au at thicknesses of about 500Å/1000Å, respectively, using e-beam evaporation.

7. The method of claim 1 wherein the ramp down in chuck bias voltage is about -200 VDC or more, the method further comprising:

depositing conformal silicon nitride for passivation of the recessed base layer;

directionally etching to remove silicon nitride on planes parallel to the n^+ GaN quasi-substrate layer;

depositing a base metallization layer; and

lifting-off base metallization, thereby forming a base contact pad.

8. The method of claim 7 wherein an anneal is performed post-base metallization so as to provide the base contact pad with low reverse current leakage and low contact resistance.

9. The method of claim 1 further comprising:

opening an emitter etch/contact window using optical lithography;

etching an emitter recess to the n^+ GaN quasi-substrate layer;

depositing an emitter ohmic metallization layer over the etched emitter recess; and

lifting-off emitter ohmic metallization, thereby forming an emitter contact pad.

10. The method of claim 1 wherein the emitter ohmic metallization layer includes at least one of titanium, aluminum, nickel, and gold.

11. The method of claim 1 further comprising:

opening a window for RF test pad metallization using optical lithography;

depositing an RF test pad metallization layer; and

lifting-off RF test pad metallization, thereby providing RF test pads.

12. The method of claim 1 wherein the helium implantation is achieved with an implant depth of about 2 μm.

13. The method of claim 1 wherein the ohmic metallization layer over the window for the collector fingers is Ti/Ni with thicknesses of 100Å and 400Å, respectively.

14. The method of claim 1 wherein the device has a plurality of collector fingers about 0.2 μm wide and having a finger pitch between 1:1 and 1:3.

15. An etched grooved GaN-based permeable-base transistor device, comprising:

a GaN emitter region having a thickness of about 6 to 10 μm, and grown on (0001) sapphire using hydride vapor-phase epitaxy (HVPE) and He implantation under base and collector contact pads at an implant angle of about 7°;

a GaN base region having a thickness of about 1 to 2 μm, and grown on the GaN emitter region using molecular beam epitaxy (MBE); and

a GaN collector region having a thickness of about 0.1 to 0.3 μm, and a plurality of collector fingers having finger sidewall angles of about 80° to 85° for 1:1 and 1:3 finger spacing, wherein the collector region is grown on the GaN base region using MBE.

16. The device of claim 1 wherein the device has ten or more collector fingers each about 0.2 μm wide.

17. The device of claim 1 wherein spacing between each collector finger is smaller than 1 μm.

18. The device of claim 1 wherein the each collector finger has two adjacent base contacts, the base contacts having a width substantially equivalent to the gate length of the device.

19. An etched grooved GaN-based permeable-base transistor device, comprising:

a GaN emitter region grown using hydride vapor-phase epitaxy (HVPE);

a GaN base region grown on the GaN emitter region using molecular beam epitaxy (MBE); and

a GaN collector region grown on the GaN base region using MBE, and having a collector pad region and a plurality of collector fingers, wherein the collector fingers have a first height in the collector pad region and a second height out of the collector pad region, with the first and second heights configured so as to prevent disconnect between the collector fingers and the collector pad region.

20. The device of claim 19 wherein the device has ten or more collector fingers each about 0.2 μm wide.

21. A method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising:

opening a window for a base recess; and

etching to recess a base layer to an n^- GaN quasi-substrate layer grown on the n^+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage.